Doc Code: AP.PRE.REQ

PTo/SB/33 (07-05)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	550-445
Application Number	10/601,575
Filed	June 24, 2003
First Named Inventor	EVANS
Art Unit	2181
Examiner	Vincent Lai

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 33,149 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1,34 ______

Signature

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August 30, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

EVANS et al

Appl. No. 10/601,575

Filed: June 24, 2003

OIPE IAP48 AUG 30 2006 PATENT & TRADEMARK OFFICE

Atty. Ref.: 550-445; Confirmation No. 8029

TC/A.U. 2181

Examiner: Vincent Lai

For: SYNCHRONISATION BETWEEN PIPELINES IN A DATA PROCESSING APPARATUS UTILIZING A SYNCHRONISATION QUEUE

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August 30, 2006

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ARGUMENTS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

All claims stand rejected as being anticipated by USP 6,240,508 to Brown. Any claim feature missing from Brown requires that the rejection be withdrawn.[1]

The claims recite a data processing apparatus with both a main processor and a coprocessor both having plural pipeline stages. Coprocessor instructions in a sequence of instructions to be executed by the data processing apparatus are routed to the coprocessor for execution. Each coprocessor instruction may be routed through both the main processor pipeline and the coprocessor pipeline, but this means that the main processor pipeline and the coprocessor pipeline need to be synchronized. Such synchronization may be achieved by passing signals with fixed timing from one pipeline to the other. As the length of pipeline processors increases, it is more difficult to achieve synchronization between pipelines using such a tightly coupled synchronization approach.

[1] It is not understood why the Examiner is maintaining the objection to Fig. 2A and to the title. The title was amended as the Examiner requested, and a copy of Fig. 2A as filed was submitted clearly showing that block labeled as MEM1 already has a reference number of 230. Accordingly, these objections should be withdrawn.

The claimed synchronization approach uses at least one synchronizing queue to couple a predetermined pipeline stage in one of the pipelines with a partner pipeline stage in the other pipeline. The predetermined pipeline stage causes a token to be placed in the synchronizing queue when processing a coprocessor instruction. The partner pipeline stage then processes that coprocessor instruction upon receipt of the token from the synchronizing queue, thereby synchronizing the first and second pipelines at crucial points but also allowing some "slack" between the two pipelines so that strict synchronization at all stages is not necessary.

Brown preserves read and write ordering in a macro-pipelined processor of the type that decouples instruction decode and instruction execution so as to allow multiple macroinstructions to exist in the pipeline at various stages of processing. See col. 3, line 50-col. 4, line 14. Figure 1 shows a macro-pipelined processor 10 with an instruction unit 22 (referred to as the I-BOX), an execution unit 23 (referred to as the E-BOX), and a memory management unit 25 (referred to as the M-BOX). See column 7, lines 24 to 41. In Brown's system, maintaining read and write ordering is essential; otherwise, access to memory is not deterministic. Col. 49, lines 51-57 explain that some memory requests may originate from the E-BOX 23 rather than from the I-BOX 22. As a result, these explicit memory requests must be synchronized with references from previous and subsequent instructions. This is achieved by providing a spec-queue 75 and a spec-queue sync counter within the M-BOX 25. The M-BOX 25 is described in more detail with reference to Figures 15 and 18. See also Brown's claim 1.

Clear Error #1: Brown Lacks A Coprocessor. The Examiner equates the claimed main processor with Brown's CPU 10 and the claimed coprocessor with Brown's additional CPU 28 shown in Figure 1. But CPU 28 is not described in Brown as a coprocessor for the CPU 10. Col. 35, lines 45-49, referred to by the Examiner, merely describe a memory ownership technique used to ensure one processor can write to a memory location before another processor

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can read from the same memory location. But a memory ownership technique is not claimed. The Examiner contends that "it is implied by a multiprocessor system that any other processors in the environment can be a coprocessor for the processor in question." Having is rely on "implications" is further evidence that the coprocessor is missing. Moreover, the contention is simply incorrect. Another more common reason to use multiple processors is to provide additional processing resources in order to improve processing throughput. In such multi-processor systems, each processor works independently of the other rather than as a coprocessor for another processor.

The Examiner also refers to the text at col. 36; line 62 to col. 37; line 3 contending that "macro-pipeline considerations mean that instructions are split up amongst different processors." The macro-pipeline is entirely contained in the CPU 10 shown in Figure 1. The referenced text describes the internal operation of the CPU 10, and has no teaching that Brown's additional CPUs 28 act as coprocessors for the CPU 10.

<u>Clear Error #2: Brown Lacks the Claimed Coprocessor.</u>

The claimed coprocessor executes coprocessor instructions appearing in "said sequence of instructions" executed by the main processor. Even if Brown's CPU 28 were erroneously considered to be a coprocessor, it does not execute CPU 28 instructions appearing in <u>the same sequence of instructions</u> executed by Brown's CPU 10. The Examiner essentially concedes this point, but references the Examiner's earlier macro-pipelining discussion. It is not understood how Brown's macro-pipelining in CPU 10 teaches that CPU 28 executes instructions within the same sequence of instructions executed by the CPU 10. Indeed, in a typical multi-processor system, the instructions executed by the CPU 28 would be different from the instructions executed by the CPU 10.

Clear Error #3: Each Coprocessor Instruction Is Not Routed Through Both Of The Main and Coprocessor Pipelines.

Claims 1 and 29 recite that each coprocessor instruction is arranged to be routed through both the first pipeline (i.e., the pipeline of the main processor) and the second pipeline (i.e., the pipeline of the coprocessor). Although admitting that Brown's instructions are issued to only one processor, the Examiner nonetheless refers to CPU 10's macro-pipeline. As explained, this macro-pipeline architecture is internal to a single CPU—CPU 10. Nowhere does Brown disclose an instruction executed by CPU 10 also being executed by CPU 28.

Clear Error #4: Brown Lacks the Claimed Synchronizing Queue.

For the claimed synchronizing queue, the Examiner refers to col.49, lines 58-60, which identifies a spec-queue 75 appearing within an M-BOX 25 of the CPU 10. The spec-queue 75 is provided *entirely within* the main processor 10 to synchronize when the E-BOX 23 can issue memory requests in addition to I-BOX 22. Accordingly, Brown's spec-queue 75 cannot be equated with the claimed "at least one synchronizing queue," because the claimed synchronizing queue "coupl[es] a predetermined pipeline stage in one of the pipelines with a partner pipeline stage in the other of the pipelines," and hence, couples a pipeline stage in the main processor with a pipeline stage in the coprocessor (or vice-versa). No such queue is described in Brown. Nor does Brown even disclose any queue *between* the CPU 10 and the CPU 28.

Clear Error #5: Brown Lacks the Claimed Token.

The Examiner tries to equate the claimed "token" with the commands associated with Brown's spec-queue 75, which is entirely internal to one CPU 10. Again, the spec-queue 75 does not act as a synchronizing queue between a processor and a coprocessor. The spec-queue commands, generated by the I-BOX and E-BOX of the CPU 10, are used to ensure that memory ordering is preserved when accessing memory. These very different tokens/ commands are not

placed in a synchronizing queue by a predetermined pipeline stage when processing a coprocessor instruction. Brown also does not teach the claimed partner pipeline stage then processing the coprocessor instruction upon receipt of the claimed token from the synchronizing queue so that the first and second pipelines are synchronized between the predetermined pipeline stage and the partner pipeline stage.

So Brown lacks coprocessor instructions from the same sequence of instructions as the main processor routed through both the pipelines of the main processor and the coprocessor. Further, Brown lacks a queue by which a synchronizing token is passed between the main processor and a coprocessor. In fact, Brown does not even consider the problem of synchronization between a main processor pipeline and a coprocessor pipeline in situations where a coprocessor instruction is routed through both pipelines. Given these five clear errors set forth above—any one of which defeats the anticipation rejection based on Brown—the final rejection should be withdrawn, and the application passed to allowance.

Respectfully submitted,

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